DESIGN AND FABRICATION OF AN F. M. TRANSMITTER

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MASTER OF TECHNOLOGY

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CERTIFICATE

Certified that this work on "Design and Fabrication of a F.M. Transmitter" has been carried out under my supervision and this has not been submitted elsewhere for a degree.

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ABSTRACT

This thesis deals with the design and fabrication of a solid state FM transmitter. It mainly concerns with the theory, design and experimental results that have been obtained by varying the junction-capacitance of a reverse biased diode, which is a part of the tank circuit of the oscillator. The frequency has been multiplied by a factor of fiftyfour to reach the desired frequency of transmission. Power output of the transmitter is supposed to be adequate to receive signals over a range of 2 KM. The novelty of the project is, that no imported component has been used and all the work has been carried out with indigenous components that are available in the Indian Market.

The transmitter set can be used at one end for short distance communication if a suitable receiver is used at the opposite end. It is helpful in Walkie-Talkie equipment because the set is completely transistorised and makes use of two six volts dry cell batteries as the power source.

CHAPTER I

INTRODUCTION

The equipment that has been fabricated is useful for short distance communications. A transmitter of centre frequency seventy MHz has been designed and fabricated. Modulation is effected by a varicap. Solid state circuitry has been employed and the components that are used are all indigenous.

Chapter two of this report deals with the theory of modulation; it has been shown how to get frequency modulation when tank circuit capacitance of the oscillator is varied in accordance with an audio signal. Audio signal varies the junction capacitance of a reverse biased diode and hence the frequency of the oscillator tank-circuit. Next, a schematic block diagram and description of different blocks is given.

In Chapter three the necessary disign data is given and also results of measurements carried out on different diodes. The measurements concern with the junction capacitance and reverse bias of the diode. A diode CD-21 is chosen and detailed measurements carried out.

Chapter four deals with the design of different blocks of the transmitter circuit, such as oscillator, frequency multipliers,R.F. amplifiers and also the coils and transformers that have been used for tank circuits and for interstage couplings. Design principles used are very simple.

Results that have been obtained are given in Chapter five. Details are given about the carrier frequency, frequency stability of the carrier, frequency deviation and the output power. They almost match with the requirements of the problem. Frequency deviation curve with respect to the reverse bias is also given.

Chapter six concludes the report.

CHAPTER II

THEORY

2.1 Statement of the Problem

To design and fabricate a transmitter with indigenous components with the following specifications:

i) Frequency seventy MHz.

ii) Power output sufficient to transmit signals upto a distance of two kilometers.

iii) Modulation F.M. with a maximum deviation of ±75 KHz.

iv) Input audio at -72 dbm (0 dbm= 1 mW).

v) Solid state circuitry with modulation effected by varicap.

2.2 Principle of Working

The principle of working has been devided into two sections. First one deals with the theory of modulation and the second one shows how it is achieved by a varicap.

2.2.1 Theory of Modulation[1]:

Generation of frequency modulated waves by varying the capacitance of the resonant oscillator circuit is as follows:

Let, $C(t)$ = variable capacitance of the resonant circuit

$$C(t) = C_o + \Delta C \text{ Sin } w_m t \qquad (2.1)$$

where,

C_o = capacitance in the absence of modulation.

ΔC = maximum change.

Instantaneous frequency $w_i(t)$ is given by

$$w_i^2(t) = \frac{1}{LC(t)} \qquad (2.2)$$

Differentiating both sides

$$2w_i(t)\, dw_i(t) = -\frac{1}{LC^2(t)} dC(t)$$

or,
$$\frac{dw_i(t)}{w_i(t)} = -\frac{dC(t)}{2C(t)}$$

Considering the variations to be small

$$\frac{\Delta w_i(t)}{w_o} = -\frac{\Delta C(t)}{2C_o} \qquad (2.3)$$

where, $\Delta C(t) = \Delta C \text{ Sin } w_m t$.

Therefore,

$$w_i(t) = w_o + \Delta w_i(t) = w_o\left(1 - \frac{\Delta C}{2C_o} \text{Sin } w_m t\right) \qquad (2.4)$$

Similarly, if C is considered to be constant and the inductance L is varied we obtain the expression

$$w_i(t) = w_o\left(1 - \frac{\Delta L}{2L_o} \text{ Sin } w_m t\right) \qquad (2.5)$$

we get,

$$w_i(t) = w_o\left(1 + \frac{\Delta w}{w_o} \text{ Sin } w_m t\right) = w_o + \Delta w \text{ Sin } w_m t$$

Negative sign in equation (2.3) shows that

a) Increasing the capacitance decreases the frequency, and

b) Decreasing the capacitance increases the frequency.

In the next sub-section we will see how we get this variation of tank capacitance from a reverse biased diode (varicap).

2.2.2 Varicap:

Here frequency modulation is obtained by varying the capacitance of the tank circuit of the oscillator in accordance with the amplitude of the audio signal. The capacitance variation of the tank circuit may be obtained in many different ways and one out of them has been employed[2].

In a junction diode if the reverse bias across the diode junction is varied, the junction capacitance also varies.

There is a dipole layer of charge in the region of any barrier, which is necessary to create the electric field in the barrier region. If the voltage is increased in the barrier region (reverse bias) the field increases in the barrier region and amount of charge in the dipole layer must also increase.

The number of ionised donors and therefore amount of positive charge found in the depletion region of the barrier is much greater for reverse-bias than for the forward bias. If the charge in the depletion region changes as the bias voltage changes, it is clear that a barrier capacity C_b must exist. The dipole layer here consists of the unneutralised ionised impurity atoms found in the depletion region of the junction barrier and since the impurities are distributed in the volume of the semiconductor, the thickness of the depletion region must always increase as the charge and voltage increase. That means junction capacitance between the terminals decreases for the reverse bias and increases with the forward bias.

Capacitance voltage characteristics of a typical varicap look as depicted in Figure 2.1.

Instantaneous change of capacitance with the applied bias voltage is the most important feature of varicaps. Capacitance as a function of bias voltage can be expressed by the following equation for a reverse biased varicap.

$$C_T = C_p + C_j = C_p' + \frac{C_{jo}}{(1 + \frac{V_{bias}}{\phi})^n} \qquad (2.6)$$

where

C_T = Total capacitance of varicap.

C_p = Package capacitance

C_j = Junction capacitance

C_{jo} = Junction capacitance at zero bias

V_{bias} = Applied reverse bias

ϕ = Contact potential (function of the semiconductor and doping level)

n = exponent of capacitance variation.

ϕ = 0.5 - 0.7 volts for silicon

= 1.1 - 1.2 volts for Gallium arsenide

n is a function of the junction type.

n = 1/2 for abrupt junctions
= 1/3 for graded junctions
} Ideally.

In actual device C-V characteristics can be approximated by using a value of n between 0.28 - 0.45. Assuming a typical capacitance-voltage function of

$$C_j = \frac{C_{jo}}{\left(1 + \frac{V_{bias}}{0.5}\right)^{1/3}} \qquad (2.7)$$

for a silicon diode.

For the experiments carried out capacitance of different diodes was measured at a number of discrete bias voltages and then best was chosen. Practically, a partial curve is used for the modulation such that it

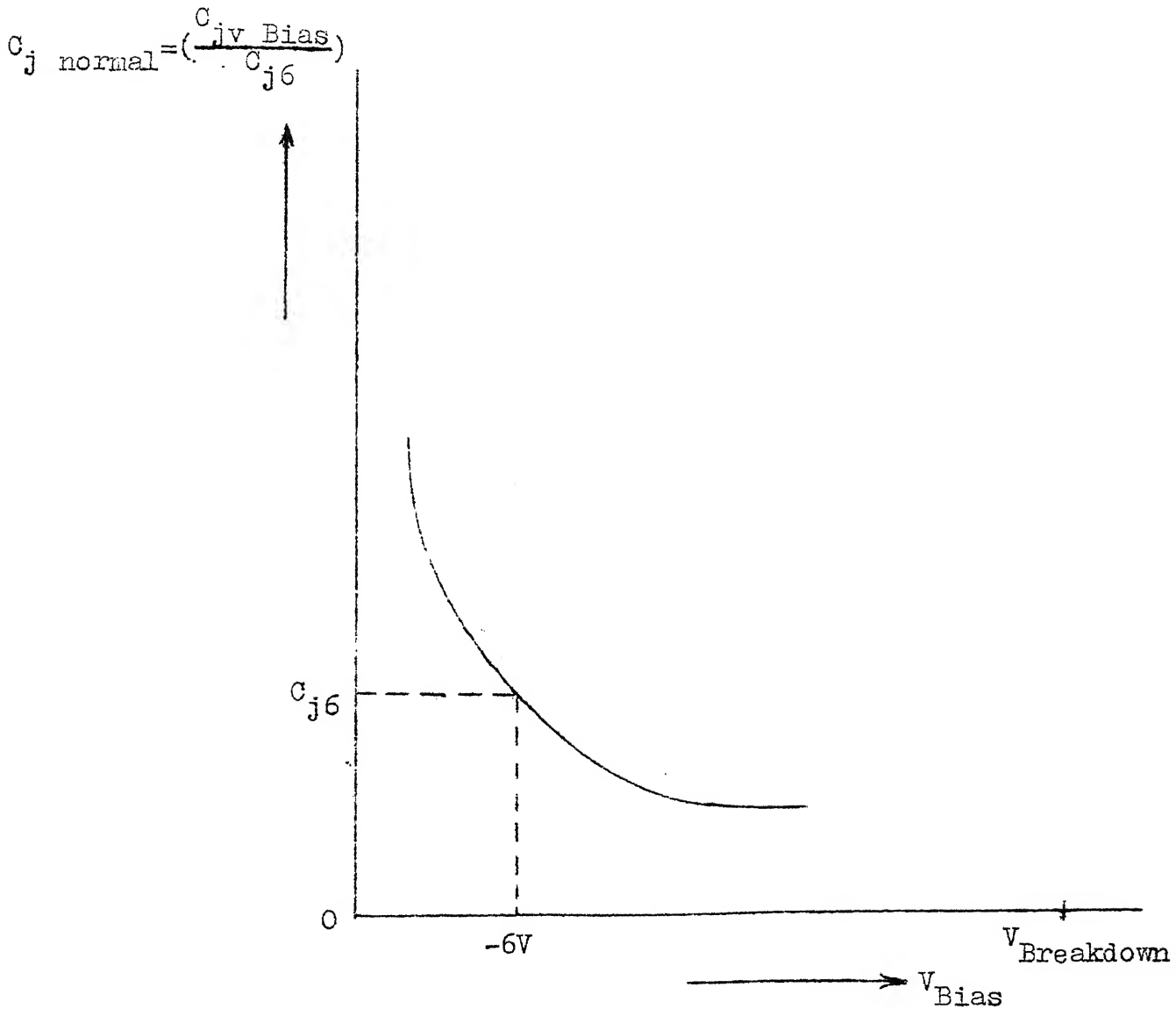


Figure 2.1: Normalised Junction Capacitance of a Typical Varicap.

gives almost a linear range of variation of capacitance with respect to reverse bias voltage.

2.3 Schematic Block Diagram

The schematic block diagram of the circuit of a suitable transmitter is given in Figure 2.2 and is described in the following pages.

2.4 Functions of Different Blocks

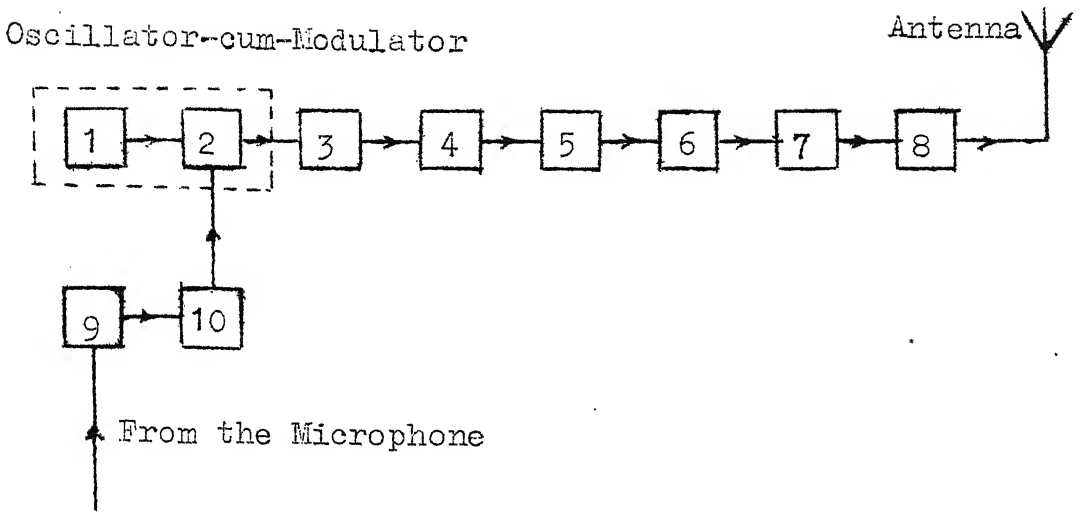
If an oscillator is designed at high frequency of seventy MHz (frequency under consideration) the oscillator will have stability problems. A slight variation in circuit components might change the working frequency by quite a lot.

Therefore, the frequency which is being generated by the oscillator, has been kept at a lower value such as 1.3 MHz; and also is being frequency modulated at this lower frequency only. Main reason being that at high frequency the tank circuit capacitance itself is very small and a variation of very small amount will be needed for the required frequency deviation to achieve, which may not be practicable.

The final frequency is obtained by using a series of class 'C' amplifiers in cascade tuned to the harmonics of the input to act as frequency multipliers.

Oscillator frequency $\simeq$ 1.3 MHz

Final frequency $\simeq$ 70.2 MHz



Block No.	Description	Frequency of operation
1	Oscillator without the tank circuit	
2	Oscillator tank circuit and Modulator circuit	1.3 MHz
3	R.F. amplifier	1.3 MHz
4	First frequency multiplier(x3)	3.9 MHz
5	Second frequency multiplier (x3)	11.7 MHz
6	Third frequency multiplier (x3)	35.1 MHz
7	Forth frequency multiplier (x2)	70.2 MHz
8	Power amplifier	70.2 MHz
9	Pre-amplifier (audio frequency)	
10	Two audio amplifier stages and a low pass filter.	

Figure 2.2: Schematic block diagram of the Transmitter.

Therefore, the multiplication factor required is fifty-four which is obtained as (3x3x3x2 = 54).

2.4.1 Oscillator-cum-Modulator:

Oscillator is of Hartley type, using the transistor in common base configuration. Feedback is given from the tapping of the tank circuit coil, which is in the collector, to the emitter through a feedback capacitor. A reverse biased diode is put in parallel with the tank-circuit of the oscillator. For achieving frequency modulation, the audio signal is fed to the reverse biased diode. This varies the junction capacitance of the diode in accordance with the amplitude of the audio signal and hence the frequency of the oscillator.

A small portion of the C-V curve of the varicap diode is made use of, such that it gives practically a linear range of variation of frequency with respect to the audio input signal. In the block diagram, block one is the oscillator without the tank circuit associated with it and block two contains the oscillator tank circuit along with the modulator circuit, consisting of diode with variable capacitance property.

2.4.2 Audio Amplifier and the Low Pass Filter:

There are three stages of amplification. First is a common collector circuit which acts as a pre-amplifier for the audio signal. Since modulation is F.M., it may be

assumed that a moving coil microphone is used (for a good quality of sound reproduction, capacitor microphone could also be used), which has -72 dbm output and has an impedance of say 600 ohms with a suitable transformer being used. Now, a common collector circuit with reasonably high impedance as compared to the microphone impedance (600 ohms with transformer) may be designed as has been done in Section 4.4.1. This circuit is indicated in block nine of the schematic block diagram figure 2.2.

Next, block number ten contains two R.C. coupled common emitter stages to amplify the audio signal to the required voltage level, which comes from the microphone through the pre-amplifier. This level needed must be proper for the reverse biasing of the diode that is put in the modulator circuit. All these have been calculated and used for design in Chapter Four.

Low pass filter is used to isolate the oscillator and audio stages such that the audio frequency signal can go to the diode (reverse biased in the tank circuit of the oscillator), but radio frequency cannot come to the audio stages, otherwise, the audio frequency signal will be superimposed by the radio frequency carrier, which is not desirable.

2.4.3 Radio Frequency Amplifier:

Since the oscillator is made to oscillate at lower voltage level, so that it may not affect the modulating circuit, we need amplification of the signal, for feeding it to the class 'C' amplifier stage, which is being used for frequency multiplication by tuning its output tank circuit to the harmonics of the input frequency.

Block three radio frequency amplifier (operating frequency 1.3 MHz) is used in common emitter configuration and under class 'A' conditions. Block eight also is in common emitter configuration under class 'C' operating conditions. The operating frequencies of blocks three and eight are approximately 1.3 MHz and seventy MHz respectively.

2.4.4 Frequency Multipliers:

These are essentially class 'C' amplifier units tuned to the harmonics of the fundamental's input frequency, which are biased at zero bias voltages, such that they operate in nonlinear range of transistor transfer characteristics.

Blocks four, five, six and seven all are in common emitter configuration. Input frequencies of these blocks are 1.3 MHz, 3.9 MHz, 11.7 MHz and 35.1 MHz respectively and the output frequencies are 3.9 MHz, 11.7 MHz, 35.1 MHz and 70.2 MHz respectively.

CHAPTER III

DATA REQUIRED FOR DESIGN

3.1 Transistor CIL 472 and CIL 911[3]

The data given for the transistors that have been used is given in Table 3.1 and also all the terms that have been used in the table are defined explicitely like, collector to base voltage, emitter to base voltage, collector current and so on.

3.2 Diodes CD-21, CD-22, CD-23, CD-31, CD-32, CD-33[4]

The data given by the manufacturer for these diodes is given in the next table, Table 3.2 and the terms are also defined as in the case of transistors like peak inverse voltage, operating current and so on.

3.3 Junction Capacitance Measurement for Different Diodes

Junction capacitance measurements are made on six diodes, that are supposed to be the best junction diodes for the purpose indicated earlier, which have been identified in Section 3.2.

Boonton capacitance bridge was used to perform the measurements. This instrument works at the frequency of 100 KHz. There is a provision for applying both the reverse and forward bias to the measuring terminals. There is also a provision for measuring the direct and indirect capacitance

Table 3.1

Transistor Data

Transistor ——→ / Specifications ↓	CIL 472	CIL 911
Application	Driver pre-amplifier	Low level, low noise amplifier
Collector base voltage, volts	25	32
Collector emitter voltage, volts	25	32
Emitter base voltage, volts	5	5
Average collector current, mA	75	60
Peak collector current, mA	150	150
Collector leakage current, μA	0.7	0.1
Total dissipation at 25°C Amb temp.mW	200	150
Transition frequency, MHz	10	350
Current gain I_c^*=1 mA, V_{ceo}^{**}=10 volts	40-150	-
I_c^*=0.1 mA, V_{ceo}^{**}=10 volts	-	40-150

* I_c - Average collector current

** V_{ceo} - Collector emitter voltage

Table 3.2

Diode Data

No.	Type*	P_{iv} volts	I_o mA	I_{fm} mA	I_R µA	P_T mW
1	CD-21	20	50	150	1	150
2	CD-22	50	50	150	1	150
3	CD-23	100	50	150	1	150
4	CD-31	20	50	150	0.1	150
5	CD-32	50	50	150	0.1	150
6	CD-33	100	50	150	0.1	150

* Silicon diodes

P_{iv} - Peak inverse voltage

I_o - Operating current

I_{fm} - Maximum forward current

I_R - Reverse current

P_T Power dissipation.

Table 3.3

Diode C-V Measurements

No.	Diode type → / Reverse bias voltage volts ↓	Junction capacitance in pF					
		CD-21	CD-22	CD-23	CD-33	CD-32	CD-31
1	0.5	41.8	41.4	28.28	28.94	29.76	31.46
2	1.0	35.0	33.82	22.10	22.76	23.24	24.74
3	1.5	31.7	29.59	18.70	19.66	20.14	21.42
4	2.0	29.2	26.74	16.84	17.60	18.05	19.34
5	2.5	27.25	25.26	16.44	17.12	17.68	18.82
6	3.0	25.80	24.56	15.38	16.01	16.52	17.71
7	3.5	24.70	23.60	14.50	15.60	15.70	16.90
8	4.0	23.70	22.64	13.84	14.53	15.00	16.05

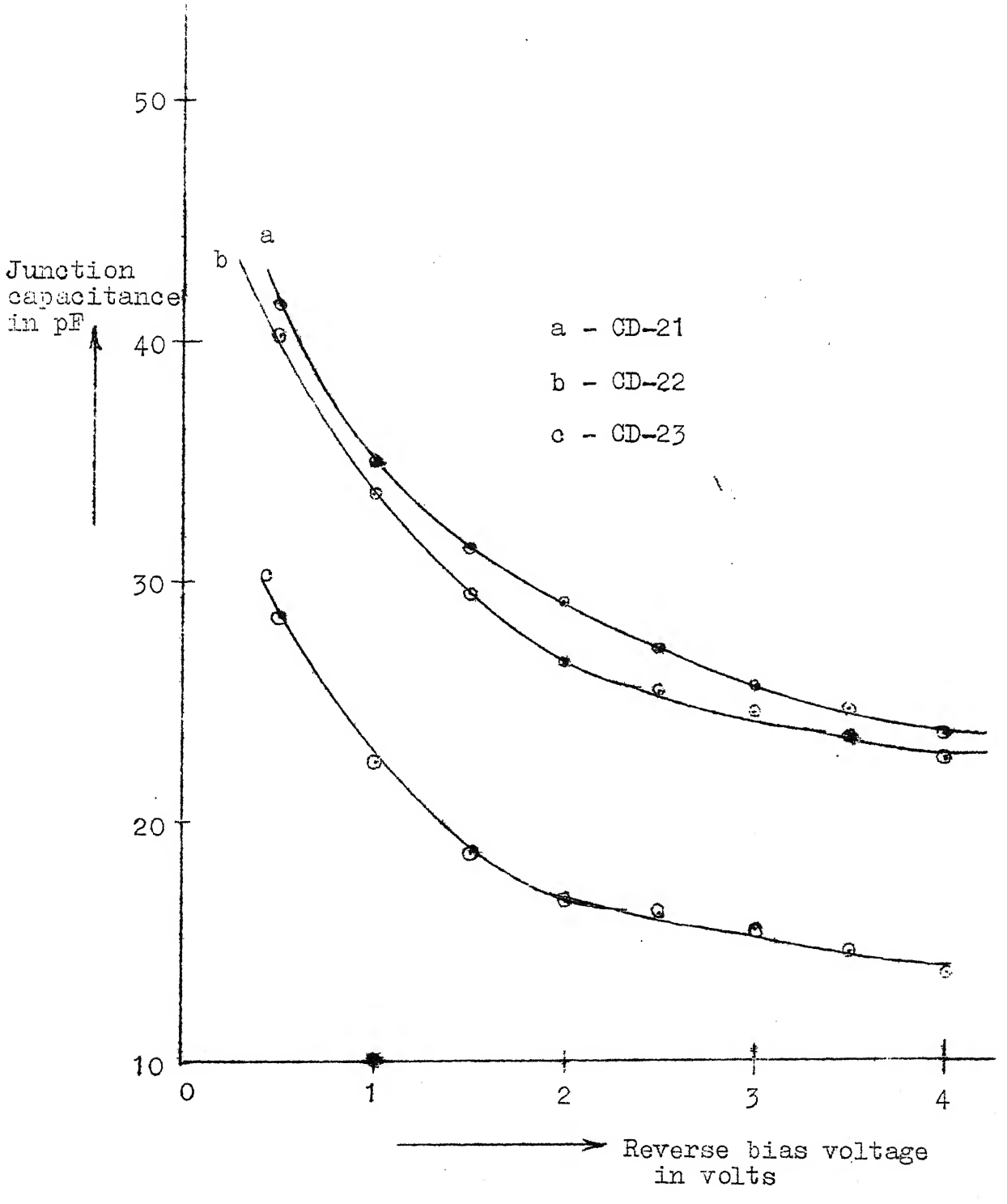


Figure 3.1: Junction Capacitance vs. reverse bias voltage curves for diodes CD-21, CD-22, and CD-23.

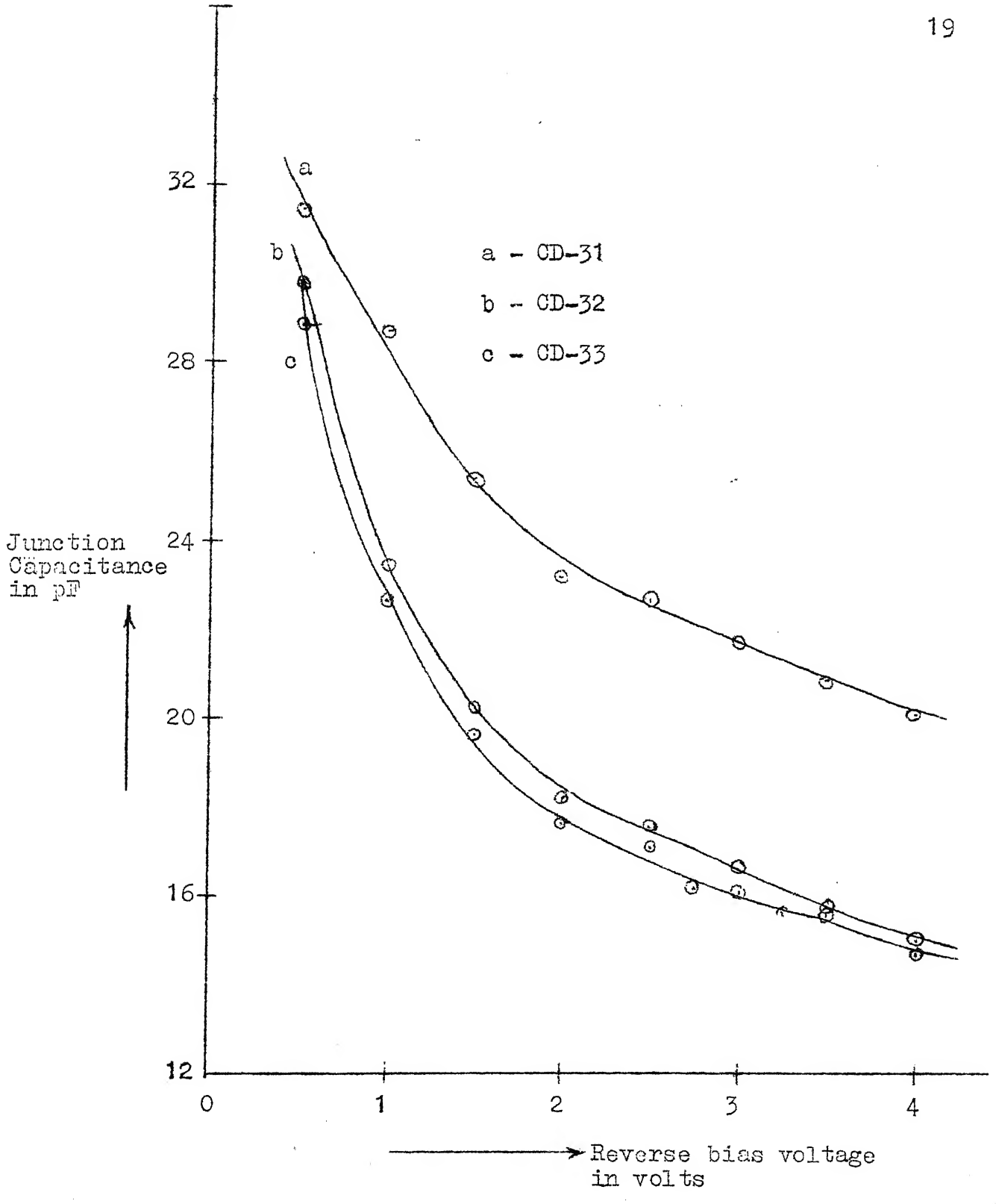


Figure 3.2: Junction capacitance vs. reverse bias voltage curves for diodes CD-31, CD-32, and CD-33.

Table 3.4

Diode Junction Capacitance vs. reverse bias voltage for CD-21

No.	Reverse bias voltage in volts	Junction capacitance pF	No. No.	Reverse bias voltage in volts	Junction capacitance pF
1	0.4	43.8	16	1.9	29.6
2	0.5	41.8	17	2.0	29.2
3	0.6	40.1	18	2.1	28.75
4	0.7	38.8	19	2.2	28.35
5	0.8	37.5	20	2.3	28.02
6	0.9	36.3	21	2.4	27.6
7	1.0	35.0	22	2.5	27.25
8	1.1	34.3	23	2.6	27.0
9	1.2	33.5	24	2.7	26.7
10	1.3	32.8	25	2.8	26.45
11	1.4	32.2	26	2.9	26.2
12	1.5	31.7	27	3.0	25.8
13	1.6	31.05	28	3.1	25.5
14	1.7	30.6	29	3.2	25.2
15	1.8	30.0	30	3.3	24.95

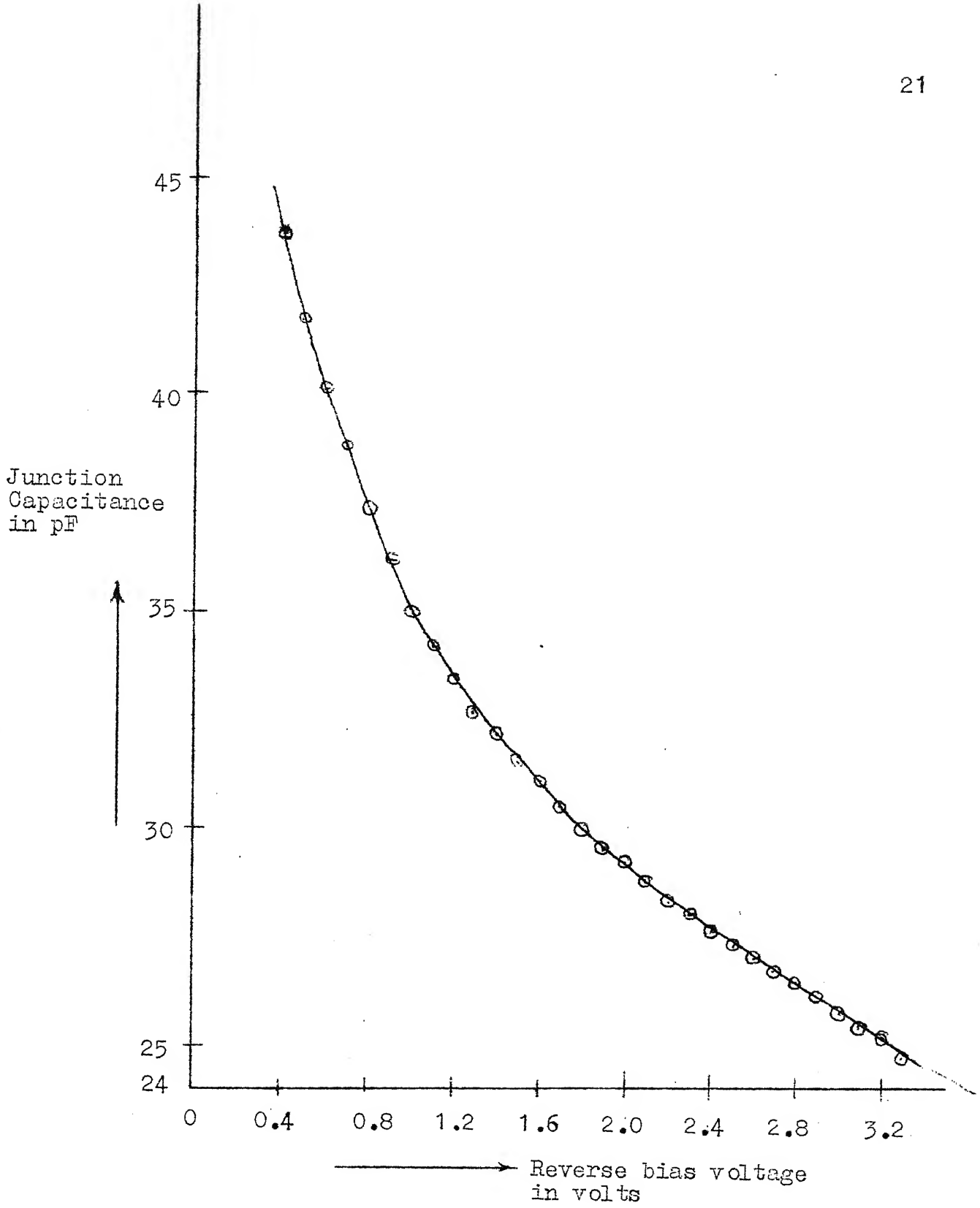


Figure 3.3: Junction Capacitance vs. reverse bias voltage curve for diode CD-21.

of the sample. Direct and indirect mean grounded and ungrounded capacitance. The diodes were connected to the instrument and the reverse bias was applied and direct capacitance (grounded capacitance) measurements were performed at different discrete bias voltages and then the curves were plotted. The results of the measurements are given in Table 3.3 and capacitance vs. reverse bias voltage curves have been plotted in Figures 3.1 and 3.2.

From the curves of junction capacitance vs. reverse bias voltage of different diodes it was found that the curves for CD-21 will give the best results out of the lot that has been taken for measurements and hence detailed measurements were made and then it was found quite suitable for the purpose of using in the circuit.

Why this particular diode was taken for the circuit will be clearer in Section 4.1. The detailed measurements are given in Table 3.4 and a precise curve has been plotted in Figure 3.3.

CHAPTER IV

DESIGN

4.1 Frequency Deviation Requirement and Choice of Diode

The desired frequency deviation at 70.2 MHz carrier is ±75 KHz as specified in the problem and then we can calculate the frequency deviation at 1.3 MHz, our starting frequency.

$$\text{Frequency Deviation at 1.3 MHz} = \pm\left(75 \times \frac{1.3}{70.2}\right) \simeq \pm 1.4 \text{ KHz}$$

Therefore frequency deviation needed at 1.3 MHz is ±1.4 KHz. Now, desired value of capacitance variation of the tank of the oscillator circuit may be calculated as follows. From equation (2.3)

$$\frac{\Delta C}{2C_o} = -\frac{\Delta w}{w_o} = -\frac{\Delta f}{f_o} \qquad (4.1)$$

where

$$\Delta f = 1.4 \times 10^3 \text{ Hz}$$

$$f_o = 1.3 \times 10^6 \text{ Hz}$$

Therefore

$$\Delta C = 2.15 \times 10^{-3} C_o$$

and $$2\Delta C = 4.3 \times 10^{-3} C_o$$

Now, to get proper amount of frequency deviation from the variation of junction capacitance of the diode we must calculate the tank circuit inductance and capacitance.

As discussed in later sections, the inductance of the tank circuit is kept at approximately 20 μH and hence the capacitance is calculated at 1.3 MHz carrier.

$$L = 20\ \mu H$$

$$f = 1.3\ MHz$$

We know,

$$f = \frac{1}{2\pi\sqrt{LC}} \qquad (4.2)$$

From this value of 'C' comes out to be approximately 749 pF by using the above equation (4.2).

Now, the required value of $2\Delta C$ may be calculated from equation (4.1) using (C_o = 749 pF).

$$2\Delta C = 4.30 \times 10^{-3}\ C_o$$

or $$2\Delta C = 3.2\ pF$$

From the curves of diodes drawn in Figures 3.1 and 3.2, it was found that, for this much of capacitance variation, the curve for diode CD-21 gives approximately a linear range of variation of 3.2 pF for reverse bias (diode biased at 1.8 volts negative) and it suits the best.

That is why, diode CD-21 was used as the circuit element for the modulator circuit.

4.2 Audio Amplitude Requirement

The bias of the diode must be such that we get practically a linear range of variation of junction

capacitance with respect to the reverse bias voltage applied. From the curve of Figure 3.3, we find that the best point for biasing it, will be approximately at 1.8 volts. At this bias a variation of 3.2 pF may be obtained by varying the bias from approximately equal to 1.5 volts to approximately equal to 2.1 volts, and therefore, the audio signal that is modulating the carrier at 1.3 MHz should be the difference of the two, peak to peak (that is approximately equal to 0.6 volts).

Now, we are in a position to calculate the gain of audio amplifier stages.

4.3 Calculation of Gain of Audio Stages

From Section 2.1 as stated in the problem Input from microphone is at -72 dbm(0 dbm= 1 mW).

$$db = 10\log_{10}(P_1/P_2) \qquad (4.3)$$

where $P_2 = 1$ mW

$$-72 = 10\log_{10}(P_1 \times 10^3)$$

From this we find that $P_1 = 63.1 \times 10^{-12}$ watts.

We have calculated the input power to the audio amplifiers through the microphone, but we want to calculate the voltage gain, which will be useful in finding out the gain of the audio stages and with the help of which then we will be able to find out the input voltage to the audio pre-amplifier.

As indicated in Section 2.4.2 we are using a moving coil type of microphone and whose impedance with suitable transformer is assumed to be 600 ohms.

Taking all these considerations into account, we can calculate the input voltage.

Power input P_1 = 63.1 pW

Impedance R = 600 ohms

Since

$$P = V^2/R \tag{4.4}$$

where P - Input power,

V - Input voltage and

R - Input resistance.

$$V = \sqrt{PxR} \simeq 0.2 \text{ mV}$$

Hence, the input voltage is 0.2 mV r.m.s approximately.

From section 4.2,

Output voltage needed = 0.6 volts peak to peak

0.6 volts peak to peak= 0.21 volts r.m.s.

Hence, the voltage gain of the audio stages is G_v and given by

$$G_v = \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{0.21x10^3}{0.2} \simeq 1,100$$

Therefore,

Voltage gain G_v = 1,100 (4.5)

This will be useful later in designing the audio stages.

4.4 Design of Audio Stages

The audio voltage gain required is approximately 1,100 as calculated in the above section. Amplifier is split into three stages, One pre-amplifier and two stages of amplification using R-C coupling. The gain adjustment may be done by a potentiometer that has been put in intermediate stage and the gain can be adjusted to a desired value.

Feedback has not been employed for simplicity of design and to avoid the complexities in calculations and performance of the amplifier stages. The design equations are very straightforward as given in later sections of this chapter.

4.4.1 Pre-amplifier Design:

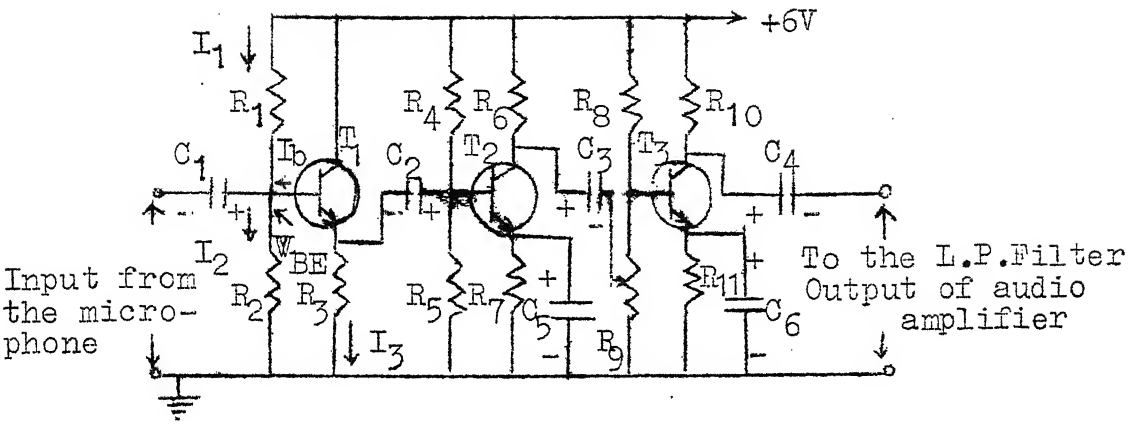
The pre-amplifier does not load the microphone connected at the input and also it isolates it. Transistor CIL 472 is used. We shall be using following biasing equations as given for a common collector circuit in Figure 4.1. According to the circuit diagram we shall be calculating the values of bias resistors and the voltages at different points.

$$I_1R_1 = (V_{CC} - V_{BE}) - (I_eR_e \text{ or } I_3R_3) \qquad (4.6)$$

$$I_2R_2 = V_{BE} + I_3R_3 \qquad (4.7)$$

$$I_1 = I_2 - I_b \qquad (4.8)$$

and Base Resistance, $R_b = R_1R_2/(R_1+R_2)$ (4.9)



R_1 = 36 K-ohms
R_2 = 12 K-ohms
R_3 = 1 K-ohm
R_4 = 51 K-ohms
R_5 = 15 K-ohms
R_6 = 4.7 K-ohms
R_7 = 1.5 K-ohms
R_8 = 51 K-ohms
R_9 = 15 K-ohms
R_{10} = 4.7 K-ohms
R_{11} = 1.5 K-ohms

C_1 = 10 μF 6V
C_2 = 10 μF 6V
C_3 = 10 μF 6V
C_4 = 10 μF 6V
C_5 = 100 μF 6V
C_6 = 100 μF 6V
$T_1 = T_2 = T_3$ = CIL472(NPN)

Figure 4.1: Audio amplifier circuit.

We are using six volts battery and therefore,

$$V_{CC} = 6 \text{ volts.}$$

For a Silicon transistor V_{BE} is of the order of 0.5 volt and therefore, we can take this approximate value for our calculations.

$$V_{BE} = 0.5 \text{ volt}$$

Assuming a reasonable current (1 mA) in the emitter and a drop of one volt across the emitter resistance R_3, such that $V_{CE} = V_{CC} - V_{R_3} = 5.0$ volts, R_3 comes out to be one kilo-ohm.

From equation (4.6),

$$I_1 R_1 = 4.5 \text{ volts} \qquad (4.6a)$$

and from equation (4.7),

$$I_2 R_2 = 1.5 \text{ volts} \qquad (4.7a)$$

For a good stability with respect to temperature variations and in turn variations in reverse collector current (I_{co}) the stability factor should be approximately 10, as given in standard text-books.

$$S \simeq 1 + \frac{R_b}{R_e} \quad \text{for } Re \gg R_b(1-\alpha) \qquad (4.10)$$

From this R_b can be calculated for

$$S = 10 \quad \text{and} \quad R_e = 1 \text{ K-ohm.}$$

It comes out as $R_b = 9$ K-ohms approximately.

Now, from equation (4.9),

$$R_b = 9 \text{ K-ohms} = R_1 R_2/(R_1+R_2) \qquad (4.9a)$$

We conveniently choose the value of R_1 and R_2 from equations (4.6a) and (4.7a).

$$I_1 R_1 = 4.5 \text{ volts}$$

$$I_2 R_2 = 1.5 \text{ volts}$$

For the convenience of calculations we can neglect I_b in comparison with I_1 and I_2 and then, we get,

$$R_1/R_2 \simeq 3 \qquad (4.11)$$

From equations (4.9a) and (4.11) we calculate the values of R_1 and R_2. They come out as

$$R_1 = 36 \text{ K-ohms}$$

$$R_2 = 12 \text{ K-ohms}$$

So, the design values for bias resistors are as follows:

$$R_1 = 36 \text{ K-ohms}, \quad R_2 = 12 \text{ K-ohms}, \quad R_3 = 1 \text{ K-ohm}$$

and also

$$V_B = \left(\frac{R_2 \parallel \beta R_3}{(R_2 \parallel \beta R_3)+R_1}\right) V_{CC} = 1.3 \text{ volts} \qquad (4.12)$$

The coupling capacitors C_1 and C_2 (at the input and output of the pre-amplifier) are designed such that they pass all the desired frequencies in the audio frequency range and disconnect the d.c. supply from going from one stage to the other. Actually, they limit the low frequency response of the amplifier and are chosen to be 10 μF in value.

Since, we are interested in voltage gain of these amplifiers, we can readily see that a common collector stage gives a voltage gain of approximately unity.

Voltage gain of an amplifier is given by[5]

$$G_v = - \frac{h_{21}/h_{11}}{y_L + h_{22}(1-S)} \qquad (4.13)$$

where, 'h_{mn}' are the 'h' parameters for the given transistor and S is the ratio ($S = h_{12}h_{21}/h_{11}h_{22}$) which is a measure of the effect that h_{12} has on the performance of the transistor. It is a measure of how much the load affects the input impedance and how much the source affects the output impedance.

Voltage gain of all three stages has been calculated in Appendix-A, by using approximate 'h' parameter of a typical low frequency, small signal transistor.

4.4.2 R-C Coupled Audio Stages:

Voltage gain of a common emitter amplifier is given by (approximately)

$$G_v = \frac{R_L \alpha}{r_e + r_b(1-\alpha)} \qquad (4.14)$$

where,

R_L = Load resistance

α = Common emitter current amplification factor

r_e = emitter resistance of the transistor

and r_b = base resistance of the transistor.

The amplifier is designed for a overall voltage gain of more than the required value (required value of voltage gain as calculated in Section 4.3 is 1,100) and then the gain is adjusted by a variable resistance as given in diagram[6] of Figure 4.1[6].

The movable element of the potentiometer is connected to the preceding stage. Thus when the gain is changed, the d.c. resistance from base to ground is maintained constant and there is no change in the bias of the stage. Since the output resistane of the preceding stage is generally, much higher than emitter, the resistance of the potentiometer or the transistor input, and the frequency response of the two stages is practically independent of the gain control setting.

Feedback is not employed in this circuit for the convenience of design and calculations and moreover without feedback also, this circuit gives quite good stability and frequency response.

Now,

V_{CC} = 6 volts

Overall desired voltage gain = 1,100

$\beta \simeq 50$

Knowing all this we will decide on the value of the biasing elements in the circuit. The design equations are as follows for Figure 4.2.

$$I_1 R_1 = V_{CC} - V_{BE} - I_3 R_3 \qquad (4.15)$$

$$I_2 R_2 = V_{BE} + I_3 R_3 \qquad (4.16)$$

$$I_1 = I_2 - I_b \qquad (4.17)$$

$$R_b = R_1 R_2 / (R_1 + R_2) \qquad (4.18)$$

$$I_6 R_6 = V_{CC} - V_{CE} - I_3 R_3 \qquad (4.19)$$

$$V_B = \frac{R_2 \,||\, \beta R_3}{(R_2 \,||\, \beta R_3) + R_1} \times V_{CC} \qquad (4.20)$$

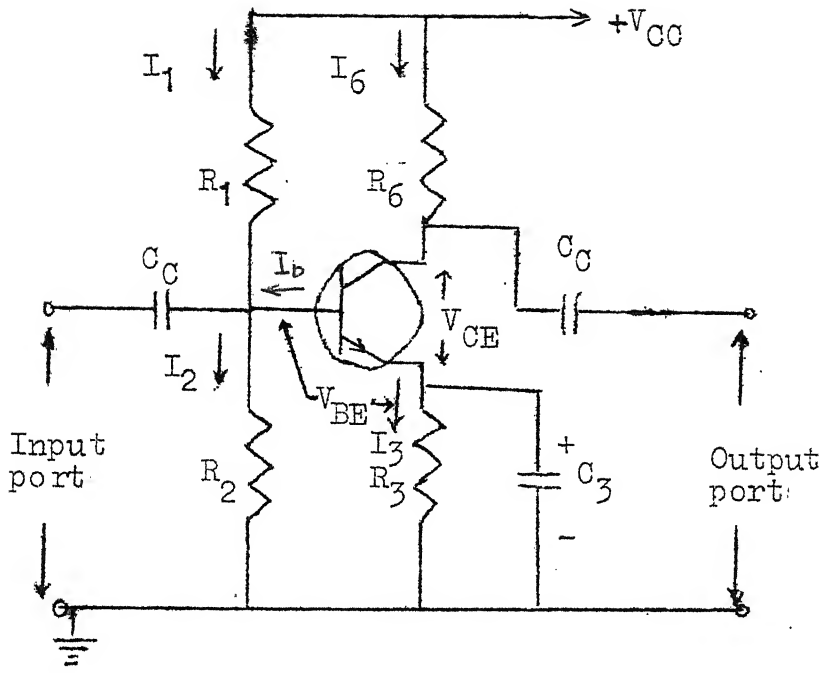


Figure 4.2: A typical single battery common emitter amplifier stage.

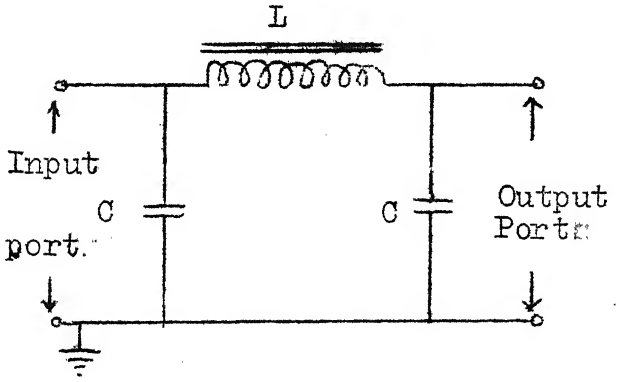


Figure 4.3: Low pass filter.

Let

V_{BE} = 0.5 V

V_{CE} = 2.25 V

I_C = 0.6 mA

and R_3 = 1.5 K-ohms

Then from equation (4.19) I_6R_6 = 2.85 volts,

and therefore R_6 4.7 K-ohms.

From equation (4.15) I_1R_1 = 4.6 volts

and from equation (4.16) I_2R_2 = 1.4 volts.

For a stability factor of 10, R_b may be chosen as 13.5 K-ohms and then the values of R_1 and R_2 may be calculated.

Neglecting the value of I_b in comparison with I_1 and I_2, we get,

$$I_1R_1/I_2R_2 = R_1/R_2 = 4.6/1.4 \simeq 3.3$$

$$\text{i.e.} \quad R_1 = 3.3\ R_2 \qquad (4.21)$$

From equations(4.18) and (4.21) we find

R_1 = 56 K-ohms, R_2 = 17 K-ohms

So, the design values of the bias resistors are as follows,

R_1 = 51 K-ohms, R_3 = 1.5 K-ohms

R_2 = 15 K-ohms R_4 = 4.7 K-ohms

and also V_B = 1.2 volts approximately.

As mentioned in previous section the voltage gain of all the three stages has been calculated in Appendix 'A' by the approximate 'h' parameters of a typical low frequency, small signal transistor.

Approximate values for gains of these two R-C coupled stages may be calculated as follows.

Stage I

R_6 = 4.7 K-ohms

and the input impedance (R_{in2}) of the next common emitter stage may be taken as 2 K-ohms then, R_L for the first stage is given by

$$R_L = R_6 \parallel R_{in2} = 1.4 \text{ K-ohms}$$

Taking the approximate values of r_e, r_b and α as

r_e = 30 ohms, r_b = 300 ohms approximately,

and $\alpha = 0.98$

Gain may be calculated from equation (4.14)

$$G_{v_1} = 38.$$

Stage II

R_6 = 4.7 K-ohms

and the input impedance of the low pass filter along with may be taken as (R_{in3} = 50 K-ohms).

R_L for the second stage = $R_6 \parallel R_{in3}$ = 4.3 K-ohms

Therefore G_{v_2} = 117.

Now, we know the approximate values of G_{v_1}, G_{v_2} and the common collector voltage gain (approximately equal to unity). Therefore, the overall voltage gain of the three stages including the pre-amplifier is

$$G_v = G_{v_1} . G_{v_2} . 1 = 4450 \text{ approximately.}$$

Then, the gain is adjusted by the potentiometer shown in Figure 4.1.

The input resistance of common emitter stages is low (generally below 5 K-ohms), large coupling capacitors C_C are used (such as 10 μF). This helps in improving low frequency response of the amplifier. The bypass capacitor C_3 in Figure 4.2 governs the low frequency response and gives a value for lower 3 db cutoff point by the formula[7]

$$f_{3db} = \frac{(\beta+1)R_E + R_i + R_T}{2\pi C_E R_E (R_i + R_T)} \qquad (4.22)$$

where

R_T - parallel combination of R_c, R_o (the output resistance of the transistor) R_a and R_b in bias circuit and R_i (the input resistance of the transistor).

From this we find that $f_{3db} = 20$ Hz

Similarly, lower 3db cutoff may also be calculated[8] for C_C. R_G is the source resistance.

$$f_{3db} = (R_3+R_i)/(2\pi C_C(R_3R_i + R_GR_3+R_GR_i)) \qquad (4.23)$$

$$= 50 \text{ Hz.}$$

A low pass filter is connected at the output of the amplifier stages, so that audio can go to the modulator, but r.f. can not come to these audio stages. This is simply a Pi-section L.C.filter with the values of L and C so that the shunt branch C offers minimum impedance for high frequencies and high impedance for low frequencies and the series branch L offers minimum impedance for low frequencies and high impedance for high frequencies. The values of L and C are

$$L = 1.5 \text{ mH}, \qquad C = 0.003 \ \mu F$$

The filter is shown in Figure 4.3.

4.5 Design of Oscillator-cum-Modulator

The oscillator designed is Hartley type[9]. Transistor CIL 911 is used as the active device for this circuit. This gives good performance at desired frequency of 1.3 MHz, because its f_T = 350 MHz. The emitter-base junction is forward biased with a (-6 volts) battery and the collector base junction is reverse biased with a (+6 volts) battery through the tank circuit coil.

Current in the emitter is kept very low so that the circuit gives oscillations of very low amplitude.

$$I_E = 0.125 \text{ mA}.$$

Therefore, the value of emitter resistance is

$$R_1 = 6/0.125 = 47 \text{ K-ohms approximately}.$$

C_3, C_5 and C_6 are the bypass capacitors, that bypass all the

r.f. whatever comes, so that it does not go into the battery.

The impedance of the capacitors is kept to be very low as compared to the parallel impedance that is going to the supply (i.e. approximately one tenth or even lower)

$$C_3 = C_5 = C_6 = 0.01 \ \mu F$$

The value of feedback capacitor C_1 and the tapping in the tank coil of the oscillator (for feedback) are chosen experimentally to give stable and sufficient amount of feedback so that the circuit oscillates at stable frequency.

R.F. Choke and L_1, L_3 are chosen so that they block the r.f. signal at 1.3 MHz and do not allow even a very small amount of signal through them.

$$L_1 = 2.0 \text{ mH}, \quad L_3 = 1.5 \text{ mH}.$$

L_1 resonates exactly at 1.3 MHz, with its self-capacitance and blocks the signal to go to the other side.

The tank circuit capacitance C_2 and inductance L_2 are designed such that they exactly resonate at 1.3 MHz when a reverse bias voltage of 1.8 volts (fixed) is applied to the diode D_1 in the modulator circuit.

Let

$$L_2 = 20 \mu H \quad \text{and} \quad f = 1.3 \text{ MHz}$$

then $$C_2 = 749 \text{ pF}$$

Capacitance C_4 is designed in a way, so that, it does not effect the tank circuit capacitance appreciably and the

variations of the junction capacitance of the diode with the variations in reverse bias on its junction. The suitable value found is

$$C_4 = 100 \text{ pF}$$

because, the junction capacitance of the diode varies in the range of 30 pF approximately.

Diode D_1 is biased at 1.8 volts reverse bias from a (-6 volts) battery. Voltage across the diode 'V_d' (Figure 4.4) is

$$V_d = 6 \times R_3/(R_2+R_3) \qquad (4.24)$$

Values of R_2 and R_3 are chosen which do not load the oscillator tank circuit and give proper value of bias.

Let

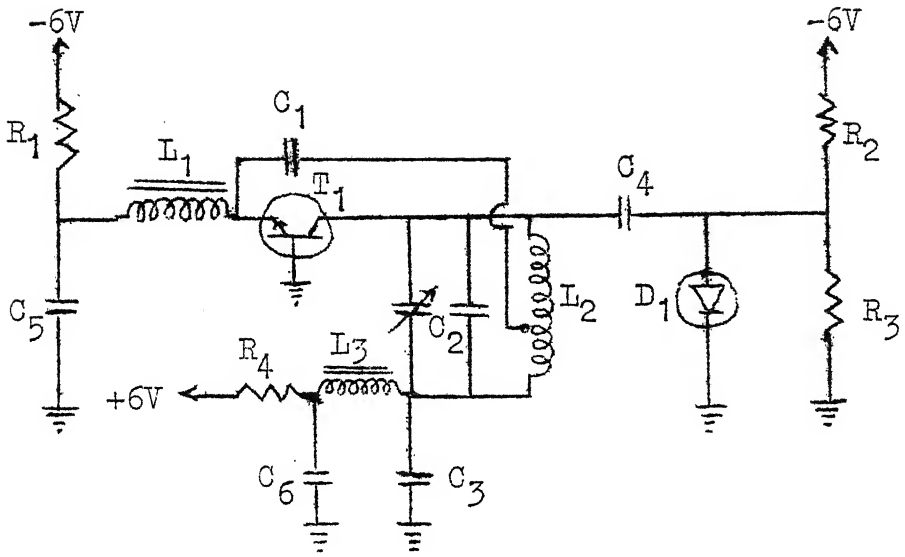
$$R_3 = 75 \text{ K-ohms}$$

and then from equation (4.24) $R_2 = 180$ K-ohms.

Diode CD-21 is used in the modulator tank circuit as discussed in previous chapter.

4.6 Design of R.F. Amplifiers

In the last section oscillator has been designed for low output voltage level, such that it does not have any adverse effect on the modulator circuit due to high amplitude of oscillations. Now since frequency is to be multiplied, the signal is to be fed to the class 'C' amplifiers (operating in the nonlinear range of the transistor) tuned to the harmonics of the input, we need



R_1 = 47 K-ohms
R_2 = 180 K-ohms
R_3 = 75 K-ohms
R_4 = 100 ohms decoupling resistor
L_1 = R.F. Choke at 1.3 MHz approximately
L_2 = Tank circuit inductance = 20 μH approximately
L_3 = R.F. Choke at 1.3 MHz approximately
C_1 = Feedback capacitor 1,000 pF
C_2 = Tank circuit capacitance = 749 pF approximately
C_3 = Bypass capacitor 0.01 μF
C_4 = Coupling capacitor 100 pF
C_5 = Bypass capacitor 0.01 μF
C_6 = Bypass capacitor 0.01 μF
T_1 = CIL-911 (NPN)
D_1 = CD-21

Figure 4.4: Oscillator-cum-Modulator Circuit.

a higher voltage than the one that is obtained from the output of the oscillator and therefore, r.f. amplifier in between the oscillator and multiplier stages.

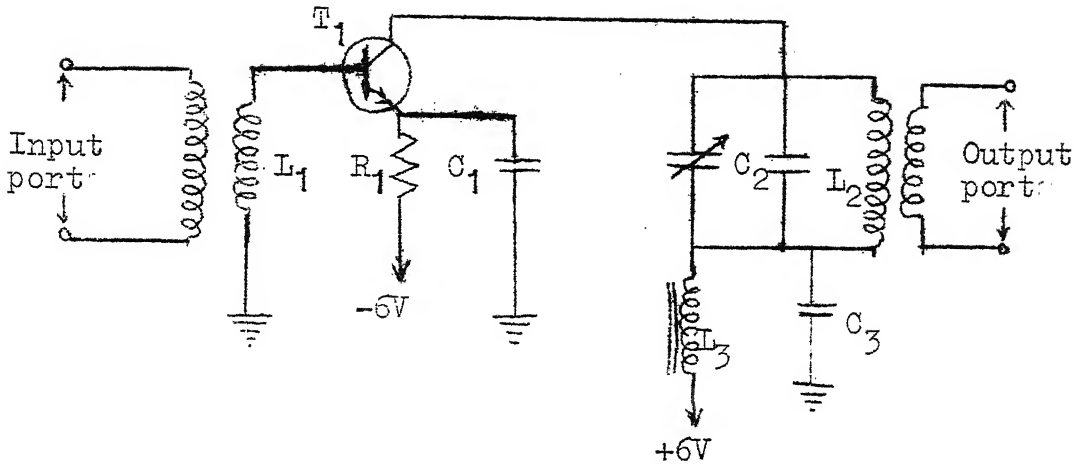
Similarly, the r.f. amplifier is also needed when the signal at the output of the last multiplier stage is very small and it is desired to transmit it to a required distance. It is not necessary that the r.f. amplifiers operate in the linear range of the transistor. The r.f. amplifiers operate in class 'C' condition to give better efficiency.

From Figure 4.5, R_1 is chosen such that a desired current is passed through the transistor. Let the emitter current is 2 mA then a value of R_1 = 5.1 K-ohms will be alright for this. A (+ 6 volts) battery is used to bias the collector in reverse bias. The tuned circuit design procedure is the same as followed for oscillator.

Table 4.1 gives the values of frequency, inductance and capacitance in the tank circuit.

As shown in Figure 4.5, variable capacitance is used in the tuned circuit to tune the tank circuit to the desired frequency.

At the end to get more power class 'C' r.f. stage is used. Its design is not at all different then the design of the last frequency multiplier stage except that only one tank circuit is used instead of two and also the neutralising circuit is not used.



R_1 = 5.1 K-phms

L_1 = Secondary of the input transformer

L_2 = Tank circuit inductance

L_3 = R.F. Choke

C_1 = Bypass capacitor 0.01 μF

C_2 = Tank circuit capacitance

C_3 = Bypass capacitor 0.01 μF

T_1 = CTL-911 (NPN)

Figure 4.5: R.F. amplifier.

4.7 Design of Frequency Multiplier Stages

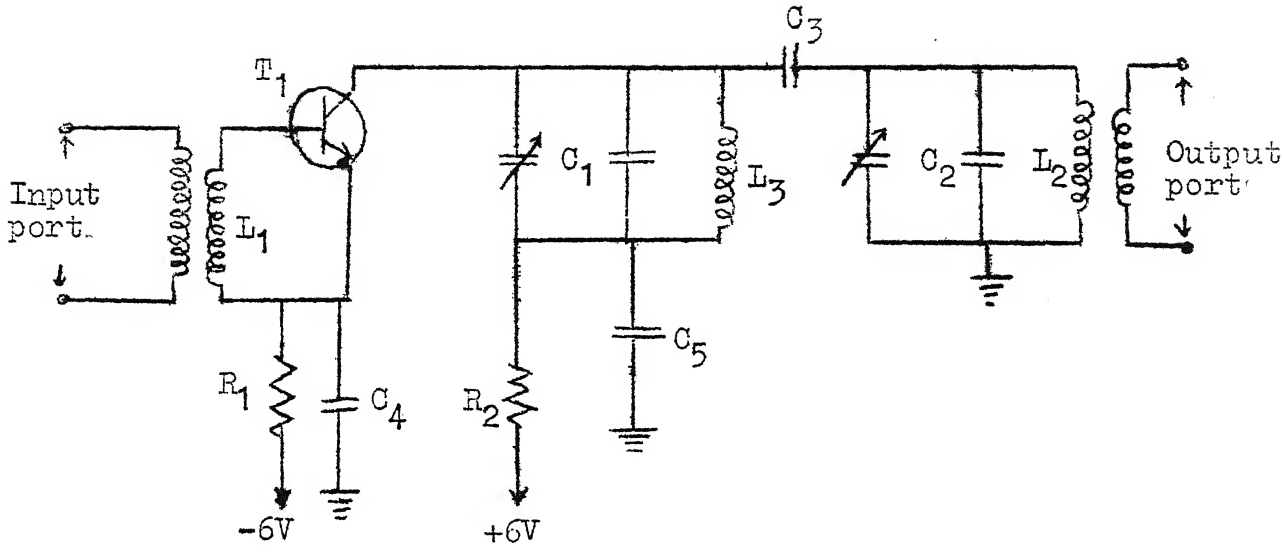
There is not much of difference in the design of frequency multipliers that have been incorporated in the R.F. amplifiers except that the multiplier is operated in class 'C' condition to give a waveform (output) less than half a cycle and the transistor is biased beyond the cutoff point of the transistor and the output tank is tuned to the harmonics of the input frequency. Collector base junction is also biased in the same way as done in r.f. amplifiers.

The value of the tank circuit components (inductance and capacitance) are given in Table 4.2. In the case of last multiplier stage neutralising is also employed as shown in the overall circuit diagram.

Design of frequency multipliers is not much involved, the only thing very important is the design of coils and transformers that are being used at the input and output of the circuit and due consideration is given to their design in the next section.

In the output tank there are two tank circuits used, employing a potential devider type of arrangement the capacitance C_3 is chosen such that it gives comparatively less admittance at the working frequency than the tank circuit.

The attenuator provided by the capacitor C_3 and the tank circuit prevents loading of the Q of the overall circuit.



L_1 - Secondary of the input transformer

L_2 - Primary of the output transformer

L_3 - Inductance of the tank circuit

C_1,C_2 - Capacitance of the tank circuit

C_3 - Potential divider capacitance

C_4,C_5 - Bypass capacitors

R_1,R_2 - Decoupling resistors

T_1 - CIL-911 (NPN)

Figure 4.6: Frequency multiplier.

Table 4.1

Tuned circuit inductances and capacitances for R.F. amplifiers.

No.	Frequency MHz	Inductance μH	Capacitance pF
1	1.3	20	749
2	70.2	0.4	13

Table 4.2

Tuned circuit inductances and capacitances for frequency multipliers.

No.	Frequency			Inductance μH	Capacitance
	Input MHz	Multiplying factor	Output MHz		
1	1.3	x3	3.9	16.7	100
2	3.9	x3	11.7	2.0	93
3	11.7	x3	35.1	0.5	41
4	35.1	x2	70.2	0.4	13

4.8 Design of Coils and Transformers

For the frequency range, that has been taken into account in this project the coils designed are all single layer solenoid type. For different frequencies, different gauge of wire has been used to give minimum losses, and a high Q and therefore a good selectivity. All the coils, including at high frequency are wound on formers in side which there is no core, because at these frequencies the losses are high which is undesirable.

The design of high frequency coils depends more on practice and experience, then on theory. For the designing of inductors at high frequency lots of empirical formulas are available in the design handbooks. However the following empirical formulae is taken into account for calculations and design of the coil.

For a single layer solenoid:[10]

$$\text{Inductance } L = \frac{0.0395\ a^2 n^2}{b} K \qquad (4.25)$$

where, n = No. of turns in the coil

a = Radius of the coil measured from the axis to the centre of the wire.

b = Length of the coil, and

K = f(2a/b) from the tables given in books, referred at the end in Bibliography.

Knowing the value of K from the table and taking all other factors into account approximate calculations were made. It is not worthwhile to give all details about the calculations in this report.

In the case of this circuit,

value of 'a' = 0.4 cm + radius of the wire

because the outer radius of the former is 0.4 cm.

The detailed data about different coils that are used in the circuit is given in Figure 4.7, and the value of the tank circuit inductances and capacitances have been put together for different circuits from Table 4.1 and Table 4.2 in the Table 4.3 for easy references.

From Figure 4.7, it is found that at some places transformer has been used for coupling to the next stage and at some places tapping is done in the primary coil itself. This is all because of practical convenience in the design and working.

The number of turns in the secondary winding are decided, having in mind the impedance matching from first stage to the next one. Following approximate data have been taken into account for the same.

Tank circuit impedance = 20 K-ohms approximately

Common emitter input impedance = 2 K-ohms approximately.

Cascading of CE to CE Configuration:

Input impedance Z_i = 2 K-ohms

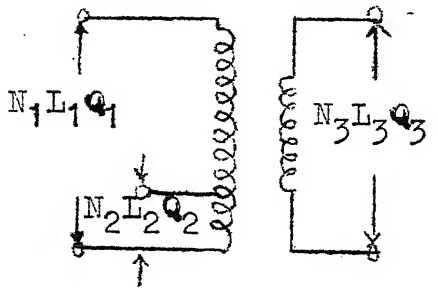
Output impedance Z_o = 20 K-ohms

$$Z_o/Z_i = 20/2 = (N_1/N_2)^2$$

Therefore, $N_1/N_2 = 3$ approximately,

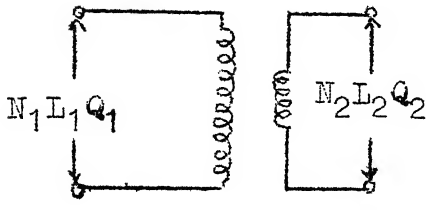
where N_1 and N_2 are the number of turns in primary and secondary of the transformer respectively.

(a) Oscillator Coil
(Wire Gauge 34SWG)



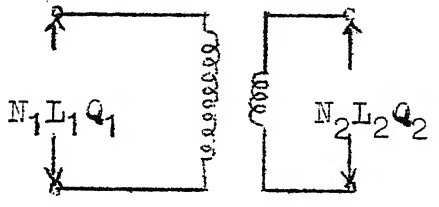
No.	N	L(/uH)	Q
1	70	20	105
2	22	4	85
3	16	2.5	60

(b) R.F.Amplifier Coil
(Wire Gauge 34SWG)



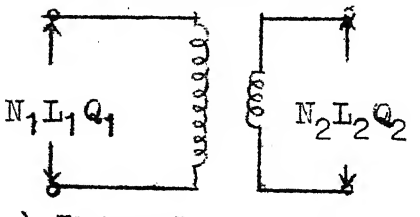
1	70	20	105
2	16	2.5	60

(c) First Frequency
Multiplier Coil
(Wire Gauge 28SWG)



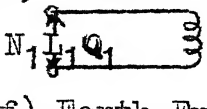
1	52	16.7	115
2	12	1.9	80

(d) Second Frequency
Multiplier Coil
(Wire Gauge 28SWG)



1	15	2.0	110
2	6	0.3	95

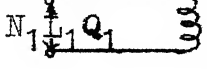
(e) Third Frequency



Multiplier coil
(Wire Gauge 20SWG)

1	8	0.5	125

(f) Forth Frequency



Multiplier and
R.F.Power Amplifier
Coils(Wire Guage
18SWG).

1	4	0.4	150

N - Number of turns, L - Inductance, Q - Quality factor of the coil.

Figure 4.7: Coil Data.

Table 4.3

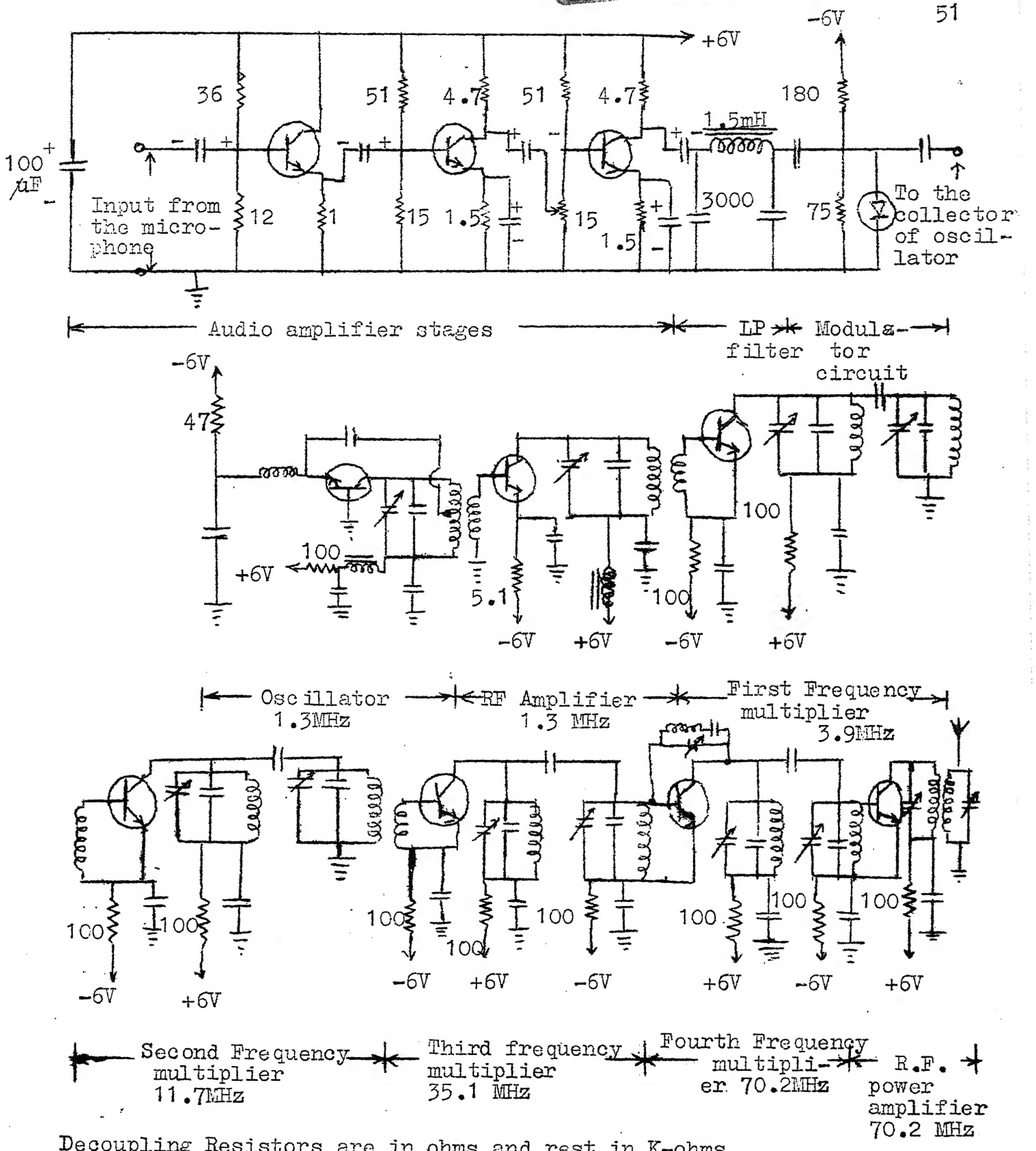
Tuned circuit inductances and capacitances for different tank circuits

No.	Circuit type	Frequency MHz	Inductance /uH	Capacitance pF
1	Oscillator	1.3	20	749
2	R.F. amplifier	1.3	20	749
3	First frequency multiplier	3.9	16.7	100
4	Second frequency multiplier	11.7	2.0	93
5	Third frequency multiplier	35.1	0.5	41
6	Forth frequency multiplier	70.2	0.4	13
7	R.F.power amplifier	70.2	0.4	13

In some cases it has not been practicable to use the same turns ratio as desired above due to practical reasons such as when already less number of turns are there in the primary.

4.9 Overall Circuit Diagram

The overall circuit diagram is shown in Figure 4.8, and the values of different components are also given near the components. Different blocks have been specified with their names, operations and operating frequencies. Different stages are coupled either by R-C coupling or by transformer or auto-transformer type of coupling. This circuit diagram can be compared to the schematic block diagram and audio and radio stages may be distinguished.



Decoupling Resistors are in ohms and rest in K-ohms.
Trimmer capacitors are 4-70 pF and all other values are given in the text.

Figure 4.8: Overall Circuit diagram of the Transmitter at 70.2 MHz.

CHAPTER V

RESULTS

5.1 Carrier Frequency and Frequency Stability

Following are the measurements made and the results of them on frequency stability.

Carrier frequency of the transmitter = 70.2 MHz approx.

Frequency stability of the carrier = $\pm$0.5 KHz approx.

All these measurements are done at the starting frequency of the transmitter and then multiplied by the proper factor. A Decade counter was used to make these measurements which goes up to 100 MHz with the plug-in-unit used. The reason for making these measurements at low frequency is that, that at high frequency the input capacitance and all other factors of the counter also come into picture thereby reducing the amplitude of the waveform and decreasing the frequency. Therefore, the measurement of frequency and its stability were done at starting point (oscillator frequency). Also the measurements of frequency deviation that are shown in the next section were done at this frequency only.

5.2 Frequency Deviation

The measurements made for frequency deviation at oscillator frequency itself are given in Table 5.1. From this table we can find out the deviation needed and adjust the audio signal accordingly such that we get ±75 KHz, frequency deviation at centre frequency of 70 MHz. The graph of this has been plotted in Figures 5.1 and 5.2.

5.3 Power Output

The required power output is actually one watt, but with the Indian transistors available, at present time (at this high frequency) this much of power cannot be attained and hence the power that is available from the transmitter is only a few tens of milliwatts.

In Appendix B a few calculations have been carried out using a formulae for transmitted power. There it has been assumed that the transmitter transmits only to area of 2 km radius around it.

As and when Indian transistors at high frequency and high power level are available, the power requirement may be fulfilled by using a power amplifier (push-pull).

From the measurements output voltage at the vertical aerial of a length of approximately equal to quarter wavelength is 3.0 volts peak to peak which comes out to be approximately 1 volt r.m.s. Therefore, the power transmitted from the antenna is approximately given

Table 5.1

Results of Frequency Measurements

No.	Reverse bias voltage in volts	Junction capacitance in pF	Frequency in KHz
1	1.1	34.3	.1297.000
2	1.2	33.5	1297.400
3	1.3	32.8	1297.800
4	1.4	32.2	1298.200
5	1.5	31.7	1298.600
6	1.6	31.05	1299.000
7	1.7	30.6	1299.500
8	1.8	30.0	1300.000
9	1.9	29.6	1300.400
10	2.0	29.2	1300.900
11	2.1	28.75	1301.300
12	2.2	28.38	1301.700
13	2.3	28.02	1302.050
14	2.4	27.60	1302.400
15	2.5	27.25	1302.800

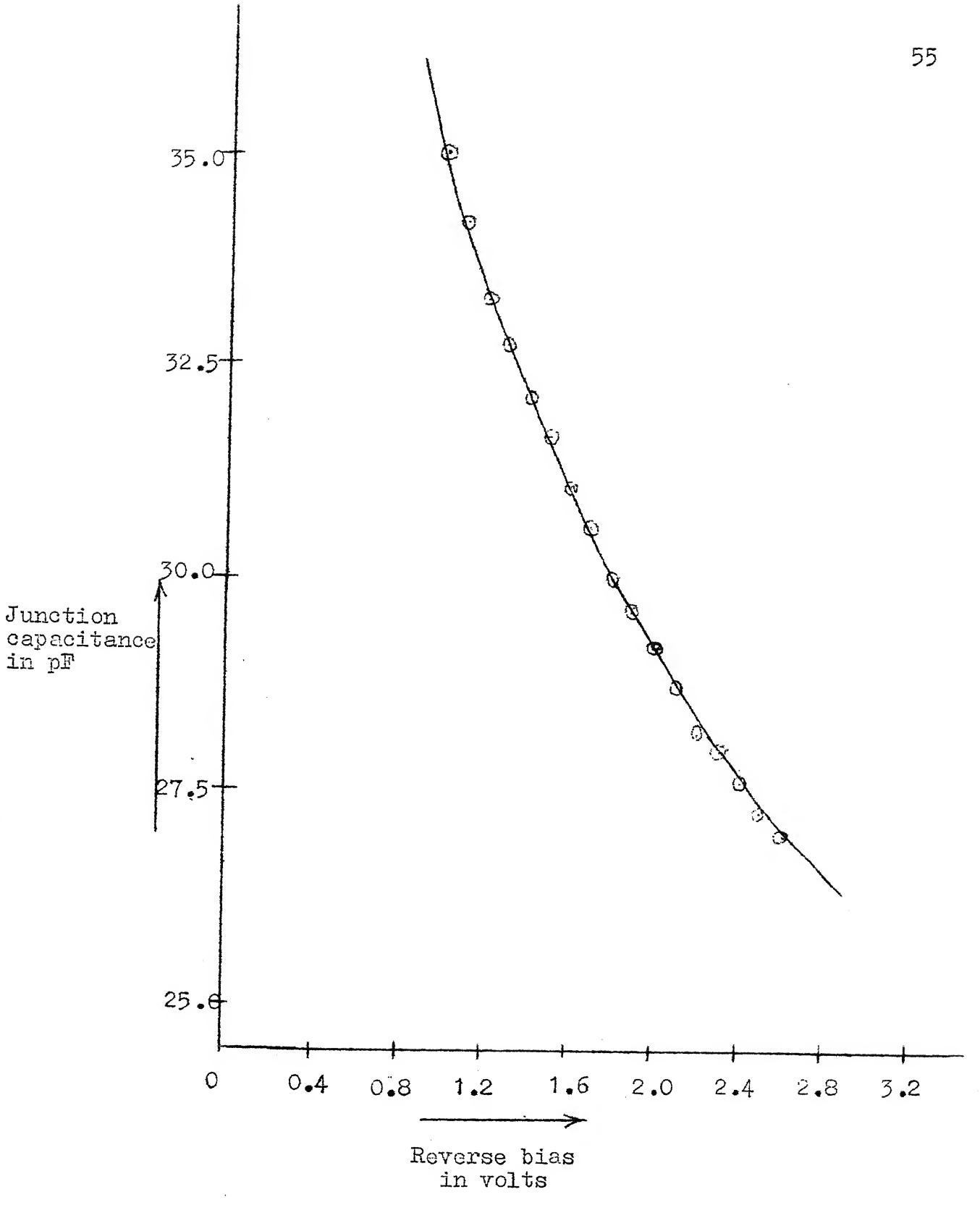


Figure 5.1: Junction capacitance vs. reverse bias voltage on the diode.

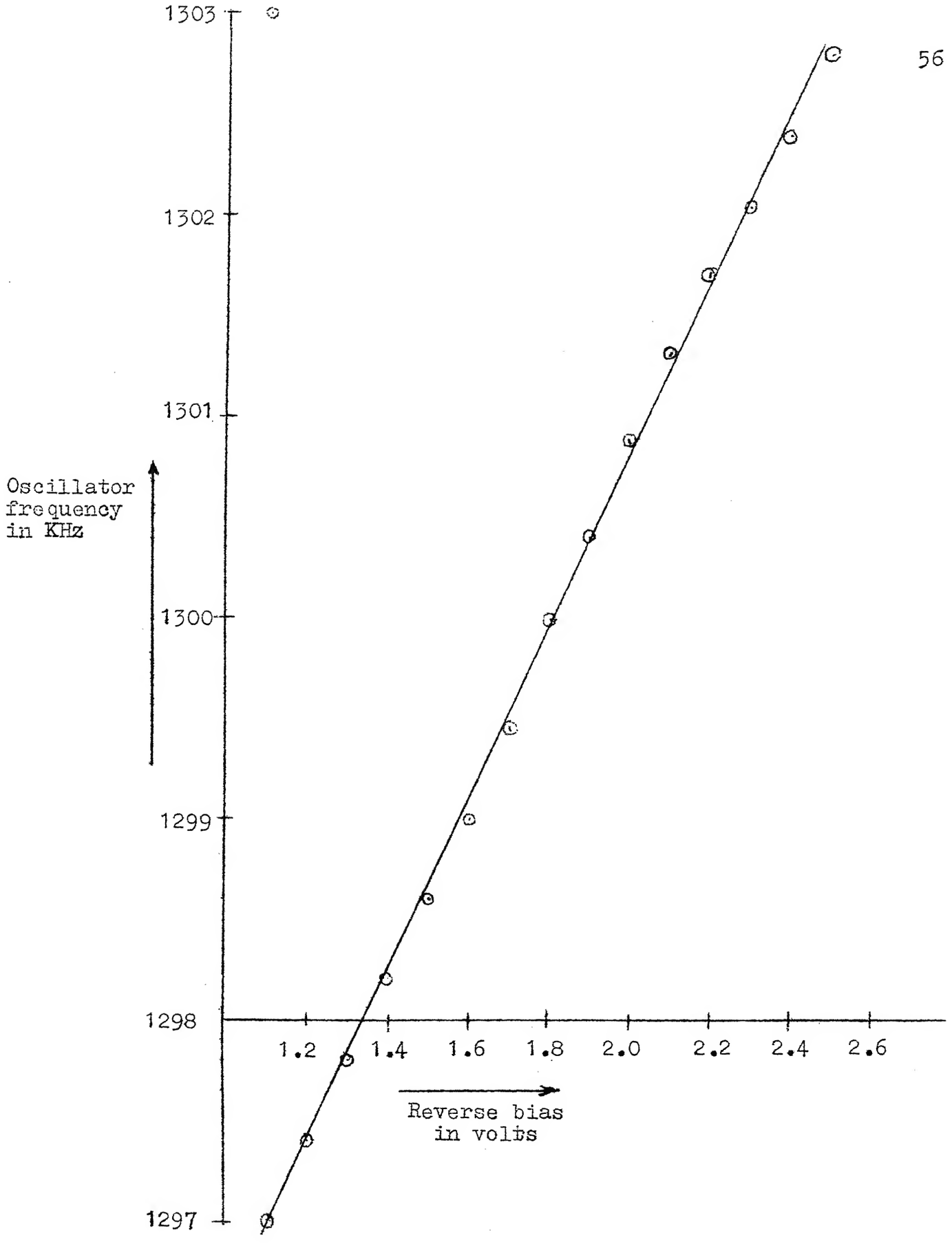


Figure 5.2: Oscillator frequency vs. reverse bias voltage on the diode.

by 1/R, where R is the radiation resistance of the antenna. Let it be 20 ohms for a quarter wave antenna then the power transmitted is 50 mW approximately which is sufficient for transmitting the signal for a distance of 2 km (Appendix B).

CHAPTER VI

CONCLUSION

The work carried out is not new but the ingenuity of the work is that, all the components that have been made use of in the circuits are indigenous.

Since variable capacitance diodes of Indian make are not freely available in the market. A simple Indian diode (junction diode) 'CD-21' from "Continental Devices" Faridabad, has been used to perform the functions of a varicap.

The original required power of 1W could not be achieved because high frequency and high power transistors that are needed to give 1W power are not available in the Indian market.

In the modulation circuit a fixed reverse bias to the diode (from a -6V battery through a potential divider arrangement) is given, which may not be suitable, because if the battery voltage drops down, the centre carrier frequency will also change. If a zener diode of suitable value is available, that can be put in this biasing circuit to get rid of this problem, then no other modification will be necessary.

Finally, a frequency of approximately 70.2 MHz has been attained and a frequency deviation of $\pm$75 KHz by adjusting the audio signal level.

APPENDIX-A

GAIN OF CASCADED AUDIO AMPLIFIERS

Here the voltage gain has been calculated for the three stage amplifier using transistor of a typical type. First of them is a common collector configuration with an unbypassed emitter resistance and the next two are common emitter stages.

The formulae for composite 'h' parameters for two cascaded stages are given below[11].

$$h_{11} = h'_{11} - \frac{h'_{12}\, h'_{21}}{1+h'_{22}\, h''_{11}}\, h''_{11} \qquad \text{(A1.1)}$$

$$h_{12} = \frac{h'_{12}\, h''_{12}}{1+h'_{22}h''_{11}} \qquad \text{(A1.2)}$$

$$h_{21} = -\frac{h'_{21}\, h''_{21}}{1+h'_{22}\, h''_{11}} \qquad \text{(A1.3)}$$

$$h_{22} = h''_{22} - \frac{h''_{12}\, h''_{21}}{1+h'_{22}\, h''_{11}}\, h'_{22} \qquad \text{(A1.4)}$$

where

h_{mn} - 'h' parameters of the two cascaded stages

h'_{mn} - 'h' parameters of the first stage

h''_{mn} - 'h' parameters of the second stage.

For a common collector stage where the emitter load impedance is unbypassed the modified 'h' parameters are given below[12].

$$h'_{11} = h_{11} + (1+h_{21})Z_e \qquad (A1.5)$$

$$h'_{12} = h_{12}\, h_{22}\, Z_e \qquad (A1.6)$$

$$h'_{21} = h_{21} \text{ approximately} \qquad (A1.7)$$

$$h'_{22} = h_{22} \text{ approximately} \qquad (A1.8)$$

where

h'_{mn} = modified parameters

h_{mn} - parameters of a common collector stage

Z_e - emitter load impedance

For a typical small signal, audio frequency amplifier transistor, 'h' parameters may be taken as below:

	Common emitter	Common collector
h_{11}	1,800 ohms	1,800 ohms
h_{12}	750×10^{-6}	1
h_{21}	49	-50
h_{22}	25 /umhos	25 /umhos
S	0.816	-1,110

Where $S = h_{12}h_{21}/h_{11}h_{22}$.

Now, from equations (A1.5) to (A1.8) parameters for a common collector stage with an unbypassed emitter load impedance (1 K-ohm approximately) may be modified and then using equations (A1.1) to (A1.4) the 'h' parameters of the three stages cascaded together (CC-CE-CE) are calculated taking two stages at a time and we get the following results for all the three stage 'h' parameters.

Parameters	CE	CC	CC with emitter load	CC with emitter load & CE	CC with emitter load & CE-CE
h_{11}	1.8	1.8	47.2	49.35	49.35 Kohm
h_{12}	750×10^{-6}	1	25×10^{-3}	22.7×10^{-6}	0.017×10^{-6}
h_{21}	49	-50	-50	23.4	1,095
h_{22}	25	25	25	25	25 μmhos
S	0.816	-1,110	1.06	0.431×10^{-3}	-12.6×10^{-6}

Now, the voltage gain is given by

$$G_v = \frac{h_{21}/h_{11}}{y_L + h_{22}(1-S)} \qquad \text{(A1.9)}$$

Letting the value of Z_L (load impedance) to be 4.3 K-ohms the gain comes out to be 4,250.

APPENDIX-B

CALCULATION OF REQUIRED POWER

The formula for Field Intensity[13] is given by

$$F = \frac{7\sqrt{P}}{d} \qquad \text{(A2.1)}$$

for a vertical aerial.

Where, F - Field Intensity in volts/meter

P - Power required in watts

d - Distance between the transmitter and the receiver in meters.

Hence, for our calculations we take the following data into account.

$F = 500\,\mu$ volts/meter

d = 2,000 meters

Now, from equation (A2.1)

$$\sqrt{P} = \frac{F\,d}{7} \qquad \text{(A2.2)}$$

From this the power required comes out to be approximately 20 mW.

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